UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,480	06/14/2001	Hsiang-Lan Lung	15313.1	8120

7590 11/16/2004

KEVIN K. JOHANSON
WORKMAN NYDEGGER & SEELEY
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UT 84111

EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,480	LUNG, HSIANG-LAN	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,22-25 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,22-25,32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: 15313.1
Filing Date: 6/14/2001
Claimed Foreign Priority Date: none
Applicant(s): Lung
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 17 filed on 10/15/2004.

Acknowledgment

1. The amendment in paper no. 17, filed on 10/15/2004, responding to the Office action in paper no. 16, mailed on 7/15/2004, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-10, 22-25, and 32-34.

Product-by-Process Claims

2. Initially, and with respect to claims 5 and 6, note that "product by process" claims are directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein that makes it clear that it is the final product *per se* which must be determined in "product by process" claims, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

> even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re*

Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that Applicant has burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 6-8, 22, 23, 25, and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US 5300799) in view of Yamauchi (US 5877054).

5. Regarding claim 1, Nakamura (see, *e.g.*, fig. 1) shows most aspects of the instant invention including a single-transistor ferroelectric memory-cell **Tr8/FC8** comprising:

- A semiconductor substrate having defined thereon:
  - A first conductive region **1** (*i.e.*, element forming region) of a first conductive type (*i.e.*, p-type). See, *e.g.*, col.3/ll.60-62.
  - A source **5** of a second conductive type (*i.e.*, n-type) defined in the first conductive region **1**, said source **5** comprising a portion of the memory cell **Tr8/FC8** and an adjacent ferroelectric memory cell **Tr7/FC7**
  - A drain **6** of a second conductive type (*i.e.*, n-type) defined in the first conductive region **1**, said drain **6** being spaced apart from sources **5** and

drains **5** of adjacent ferroelectric memory cells **Tr1/FC1-Tr7/FC7**, and wherein said drain **6** is not shared with the adjacent ferroelectric memory cells

- A channel region comprising a portion of the first conductive region that is between the source **5** and the drain **6**

➢ A gate oxide layer **7** disposed on the substrate covering the entirety of the drain **6**, channel region, and source **5**

➢ A ferroelectric gate unit **FC8** positioned on the gate oxide layer **7** comprising:

- A bottom electrode **10** in electrical communication with the drain **6**
- A top electrode **12**
- A ferroelectric layer **11** disposed between the bottom **10** and top **12** electrodes
- A sealing layer **13** disposed on each side of the gate unit **FC8**

➢ An upper conductive layer **14** disposed on the gate unit **FC1** and a portion of the gate oxide layer **7** such that the upper conductive layer **14** and the top electrode **12** of the gate unit **FC8** are in electrical communication (see, *e.g.*, col.5/ll.47-60)

Nakamura, however, fails to show the gate unit overlying a relatively larger portion of the drain than the source. Yamauchi (see, *e.g.*, figs. 25-28 and col.20/ll.28-37), on the other hand, teaches that doing so will improve the reliability of Nakamura's memory cell.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have Nakamura's gate unit overlying a larger portion of the drain than the source, as suggested by Yamauchi, to improve the reliability of the memory cell.

6. Regarding claim 4, Nakamura shows the memory cell further comprising a lower polysilicon layer **8** between the gate oxide layer **7** and the bottom electrode **10**, the lower polysilicon layer **8** doped to a conductive state (see, *e.g.*, fig. 1 and col.4/ll.33-37). Nakamura, however, fails to specify the thickness of the polysilicon layer. Nonetheless, the specific thicknesses claimed by the applicant, *i.e.*, 500-700 angstroms, absent any criticality, are only considered to be the "optimum" thicknesses of the lower polysilicon layer disclosed by Nakamura that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see, *e.g.*, Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained as long as a lower polysilicon layer is used, as already suggested by Nakamura.

In conclusion, since the applicant has not established the criticality (see next paragraph) of the thicknesses stated, it would have been obvious to one of ordinary skill in the art to use these values in the device of Nakamura.

CRITICALITY

7. The specification contains no disclosure of either the critical nature of the claimed thicknesses or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. Regarding claim 6, Nakamura (see, *e.g.*, col.4/ll.43-45) shows the source and drain regions include As ions implanted therein.

As to the method of implanting the ions, this is an intermediate process step that does not affect the structure of the final device. See, *e.g.*, MPEP § 2113, which discusses the handling of product-by-process claims.

9. Regarding claim 7, Nakamura (see, *e.g.*, col.4/ll.53-64 and col.5/ll.5-11) shows that the bottom and top electrodes may be made of Pt and that the bottom electrode may be 1000 angstroms thick. Nakamura, however, fails to specify the thickness of the top electrode. With respect to the thickness of the top electrode, see the comments stated above in paragraphs 6-7 regarding claim 4, which are considered repeated here.

10. Regarding claim 8, Nakamura shows that the ferroelectric layer may be a Pb(Zr,Ti)O3 layer, which may be about 3000 angstroms thick. Nakamura fails to show that the ferroelectric layer may have the claimed thickness of 2000 angstroms. Nonetheless, 2000 angstroms is close enough to 3000 angstroms that one of ordinary skill in the art would have expected Nakamura's ferroelectric layer to have the same properties if made having a thickness of 2000 angstroms. This is supported by the fact that the applicant is claiming the same material (*i.e.*, PZT), for the same use (*i.e.*, as a dielectric capacitor), and in the same configuration (*i.e.*, in a ferroelectric gate unit of a ferroelectric memory cell), as that of Nakamura's ferroelectric layer. See also comments stated above in paragraphs 6-7 regarding claim 4, which are considered repeated here.

11. Regarding claim 22, Nakamura (see, *e.g.*, fig. 1) shows most aspects of the instant invention including a ferroelectric memory cell **Tr8/FC8** comprising:

- A semiconductor substrate **1** having:
  - A source **5**
  - A drain **6** that is spaced apart from the source and from drains **5** and sources **5** of adjacent ferroelectric memory cells **Tr1/FC1-Tr7/FC7**, wherein the drain **6** is not shared with the adjacent ferroelectric memory cells
  - A channel defined between the source **5** and the drain **6**
- A gate oxide **7** covering the drain **5**, source **5**, and channel
- A ferroelectric gate unit **FC1** positioned on the gate oxide **7** comprising:
  - A top electrode **12**
  - A layer of ferroelectric material **11**
  - A bottom electrode **10**
- Means for controlling the polarization of the ferroelectric layer (see, *e.g.*, col.5/ll.47-60)

Nakamura, however, fails to shows the gate unit overlying the entirety of the drain and only a portion of the source. Yamauchi (see, *e.g.*, figs. 25-38 and col.20/ll.28-37), on the other hand, teaches that doing so will improve the reliability of Nakamura's memory cell.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have Nakamura's gate unit overlying the entirety of the drain and only a

portion of the source, as suggested by Yamauchi, to improve the reliability of the memory cell.

12. Regarding claim 23, Nakamura (see, *e.g.*, col.5/ll.47-67) shows that the means for controlling the polarization of the ferroelectric layer comprises an electrical connection between the drain and the bottom electrode of the gate unit.

13. Regarding claim 25, Nakamura (see, *e.g.*, fig. 1) shows the memory cell further comprising a lower polysilicon layer **8** disposed between the gate unit **FC8** and the gate oxide **7**.

14. Regarding claim 32, Yamauchi (see, *e.g.*, fig. 28) shows a gate unit positioned such that asymmetric source and drain regions are defined.

15. Regarding claims 33 and 34, Nakamura (see, *e.g.*, fig. 1) shows most aspects of the instant invention including a ferroelectric memory cell comprising:

- A semiconductor substrate comprising:
  - A source **5**
  - A drain **6** in a spaced apart configuration with respect to the source **5,** and drains **5** and sources **5** of adjacent ferroelectric memory cells **Tr1/FC1-Tr7/FC7**, wherein the drain **6** is not included as a component of an adjacent ferroelectric memory cell
  - A channel
- A gate oxide **7** substantially covering the drain **6**, source **5**, and channel
- A ferroelectric gate unit **FC8** positioned on the gate oxide layer **7**comprising:
  - A bottom electrode **10** in electrical communication with the drain **6**

- A top electrode **12**
- A ferroelectric layer **11** disposed between the bottom **10** and the top electrode **12**
- A sealing layer **13** disposed on each side of the gate unit **FC8**

➢ An upper conductive layer **14** disposed on the gate unit **FC1** and a portion of the gate oxide layer **7** such that the upper conductive layer **14** and the top electrode **12** of the gate unit **FC8** are in electrical communication (see, *e.g.*, col.5/ll.47-60)

Nakamura, however, fails to shows that the gate unit asymmetrically overlies the entirety of the drain with respect to the source. Yamauchi (see, *e.g.*, figs. 25-28 and col.20/ll.28-37), on the other hand, teaches that doing so will improve the reliability of Nakamura's memory cell.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have Nakamura's gate unit asymmetrically overlying the entirety of the drain with respect to the source, as suggested by Yamauchi, to improve the reliability of the memory cell.

16. Claims 2 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura/Yamauchi in view of Hoshiba (US 5506748).

17. Regarding claims 2 and 24, Nakamura/Yamauchi shows most aspects of the instant invention (see, *e.g.*, paragraphs 5-15 above). Nakamura (see, *e.g.*, col.5/ll.27), however, differently shows that the upper conductive layer is made out of Al-Si instead

of doped polysilicon. Nonetheless, doped polysilicon and Al-Si are known equivalents in the art for their use as conductive layer materials (see, *e.g.*, Hoshiba/col.4/ll.36-45).

Consequently, it would have been obvious at the time of the invention to use either polysilicon or Al-Si to make Nakamura/Yamauchi's upper conductive layer since, as taught by Hoshiba, these materials are known in the semiconductor art as equivalents for their use in conductive layers and selecting any of these to make Nakamura's upper conductive layer would be within the level of ordinary skill in the art.

18. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura/Yamauchi in view of Krivokapic (US 6100558).

19. Regarding claim 3, Nakamura/Yamauchi shows most aspects of the instant invention (see, *e.g.*, paragraphs 5-15 above). Nakamura also shows (see, *e.g.*, fig. 1) the memory cell comprising a plurality of LOCOS isolation fields **2** in the substrate, but fails to show a plurality of shallow trench isolation trenches (STIs).

Krivokapic (see, *e.g.*, col.5/ll.12-16) teaches that LOCOS isolation fields occupy a great deal of substrate area. STIs, on the other hand, provide for an alternative isolation technique.

It would have been obvious at the time of the invention to substitute Nakamura/Yamauchi's LOCOS isolation fields for STIs, as suggested by Krivokapic, to reduce the amount of surface area covered by the LOCOS isolation fields.

20. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura/Yamauchi in view of Jaeger.

21. Regarding claim 5, Nakamura/Yamauchi shows most aspects of the instant invention (see, *e.g.*, paragraphs 5-15 above) except for B and/or BF_2 ions implanted in the first conductive region. Nakamura (see, *e.g.*, fig. 1), however, shows that the first conductive region is of a p-type conductivity. According to Jaeger (see, *e.g.*, pp.79/ll.26), B is the only commonly used p-type dopant.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art that the p-type region of Nakamura should include B ions since, as taught by Jaeger, B is the only commonly used p-type dopant.

As to the method of implanting the ions, this is an intermediate process step that does not affect the structure of the final device. See, *e.g.*, MPEP § 2113, which discusses the handling of product-by-process claims.

22. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura/Yamauchi in view of Takenaka (US 6339008).

23. Regarding claim 9, Nakamura/Yamauchi shows most aspects of the instant invention (see, *e.g.*, paragraphs 5-15 above). Nakamura (see, *e.g.*, col.4/ll.48-52), however, shows a PSG sealing layer instead of a Si_3N_4 or an Al_2O_3 layer. Nonetheless, PSG and Si_3N_4 are known in the art as equivalents for their use as sealing layer materials (see, *e.g.*, Takenaka/col.4/ll.5-7).

Consequently, it would have been obvious at the time of the invention to use either PSG or Si3N4 to make Nakamura/Yamauchi's sealing layer since, as taught by Takenaka, these materials are known in the semiconductor art as equivalents for their

use in sealing layers and selecting any of these to make Nakamura's sealing layer would be within the level of ordinary skill in the art.

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura/Yamauchi in view of Schmidt (US 6172392).

25. Regarding claim 10, Nakamura/Yamauchi shows most aspects of the instant invention (see, *e.g.*, paragraphs 5-15 above). Nakamura, however, fails to specify a thickness of 0.18-0.35 μm for the top electrode. With respect to the thickness of the channel, see the comments stated above in paragraphs 6-7 regarding claim 4, which are considered repeated here.

In spite of the above, Schmidt (see, *e.g.*, col.1/ll.16-23) teaches that the semiconductor processing-technology has progressively moved toward defining smaller features, characterized by transistors with a channel length of 0.18 μm. As feature size shrinks, the density of the resulting circuit increases.

Consequently, it would have been obvious to one of ordinary skill in the art that the channel length of the memory cell of Nakamura should have a channel length of about 0.18 μm, as taught by Schmidt, since channel lengths of 0.18 μm are a characteristic feature of the semiconductor technology at the time of the invention that strives to increase circuit densities.

Response to Arguments

26. The applicant argues:

The amended claims require in a single transistor ferroelectric memory cell, the presence of a semiconductor substrate having a source, and a drain that is spaced apart from the source. The drain is also being claimed as spaced apart from sources and drains of adjacent ferroelectric memory cells, wherein said drain is not shared with adjacent ferroelectric memory cells. Neither Nakamura nor Yamauchi disclose such a memory cell structure.

The examiner responds:

Nakamura clearly shows these features of the claimed invention. See, for example, fig. 1, where Nakamura shows, in a single transistor ferroelectric memory cell **Tr8/FC8**, the presence of a semiconductor substrate **1** having a source **5**, and a drain **6** that is spaced apart from the source **5**. The drain **6** is spaced apart from sources **5** and drains **5** of adjacent ferroelectric memory cells **Tr1/FC1-Tr7/FC7**, and the drain **6** is not shared with the adjacent memory cells.

27. The applicant argues:

> Nakamura teaches away from Yamauchi. In detail, the attached drain and source of Yamauchi are respectively associated with distinct memory cells (Yamauchi/col.12/ll.9-13), while the source/drain diffusion regions of Nakamura are commonly shared between adjacent memory cell transistors (Nakamura/col.2/ll.42-44, col.3/ll.65-66).

The examiner argues:

Yamauchi differently teaches in the section quoted by the applicants, *i.e.*, Yamauchi/col.12/ll.7-20, that the source/drain diffusion regions are shared between adjacent memory cells, same as Nakamura (see also Yamauchi/figs. 1 and 2A and Nakamura/fig. 1).

Conclusion

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

30. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 872-9306**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

32. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

33. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/295,314-326,389; 438/3,279; 365/145	11/4/2004
Other Documentation: PLUS Analysis	9/14/2002
Electronic Database(s): EAST (USPAT, EPO, JPO, PGPub)	11/4/2004

LONG PHAM
PRIMARY EXAMINER

Marcos D. Pizarro-Crespo
Patent Examiner
Art Unit 2814
571-272-1716
marcos.pizarro@uspto.gov

MDP/mdp
November 4, 2004